30. (Amended) An integrated circuit package comprising:

a first conductive layer having a first grid of holes disposed relative to a first coordinate system;

a second conductive layer parallel to the first conductive layer, the second conductive layer having a second grid of holes offset from the first grid of holes and disposed relative to the first coordinate system; [and]

a dielectric layer between the first and second conductive layers; and

at least one conductive signal trace disposed within the dielectric layer, the at least one conductive signal trace disposed parallel to an axis of a second coordinate system that is rotated with respect to the first coordinate system by an angle of between zero and forty-five degrees.

31. (Cancelled) The integrated circuit package of claim 30 further comprising a signal layer embedded in the dielectric layer.

32. (Cancelled) The integrated circuit package of claim 31 wherein the signal layer includes at least one signal trace.

34. (Cancelled) The integrated circuit package of claim 32 wherein the first and second grids of holes have an x direction and a y direction, neither of which being parallel to the at least one signal trace.

35. (Amended) The integrated circuit package of claim 34 wherein the at least one conductive signal trace includes at least one segment rotated substantially 22.5 degrees relative to the first coordinate system[x direction] .

37. (Amended) The integrated circuit package of claim 30 wherein the first grid of holes includes holes spaced with non-equal pitch in an x direction and in a y direction relative to the first coordinate system.